Amendments to the Claims

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

Listing of Claims

1. - 9. (cancelled)

10. (new) A semiconductor device comprising:

a plurality of memory mats each of which includes a plurality of memory cells adapted to store an information code or an error correcting code for the information code;

an information storing part which includes the plurality of memory mats;

an error correcting circuit adapted to correct an error of the information code stored in the information storing part by using the error correcting code and adapted to correct the information code by one correction unit of a predetermined number of information codes;

wherein the semiconductor memory device is adapted to include a parallel test mode which activates and tests the plurality of memory mats simultaneously and which is a different function from a normal read or write function which activates one of the plurality of memory mats,

wherein the semiconductor memory device further includes parallel decision circuits which are adapted to be activated during the parallel test mode and which are respectively coupled between the error correcting circuit and each of the plurality of the memory mats, and

wherein the parallel test circuits are adapted to detect a one bit information code defect by the correction unit during the parallel test mode.

11. (new) A semiconductor device according to claim 10,

wherein the parallel test circuits are adapted to decide that the one bit information code defect is an acceptance decision, and

wherein the parallel test circuits are adapted to decide that all bits information code coincidence is also an acceptance decision,

12. (new) A semiconductor device according to claim 10,

wherein the parallel test circuits are adapted to decide that the one bit information code defect in all bits or a two bit information code defect in all bits which exists in a different correction unit are acceptance decisions.

13. (new) A semiconductor device according to claim 11,

wherein the acceptance decisions assume relief in the error correction by the error correcting circuit.

14. (new) A semiconductor device according to claim 12,

wherein the acceptance decisions assume relief in the error correction by the error correcting circuit.